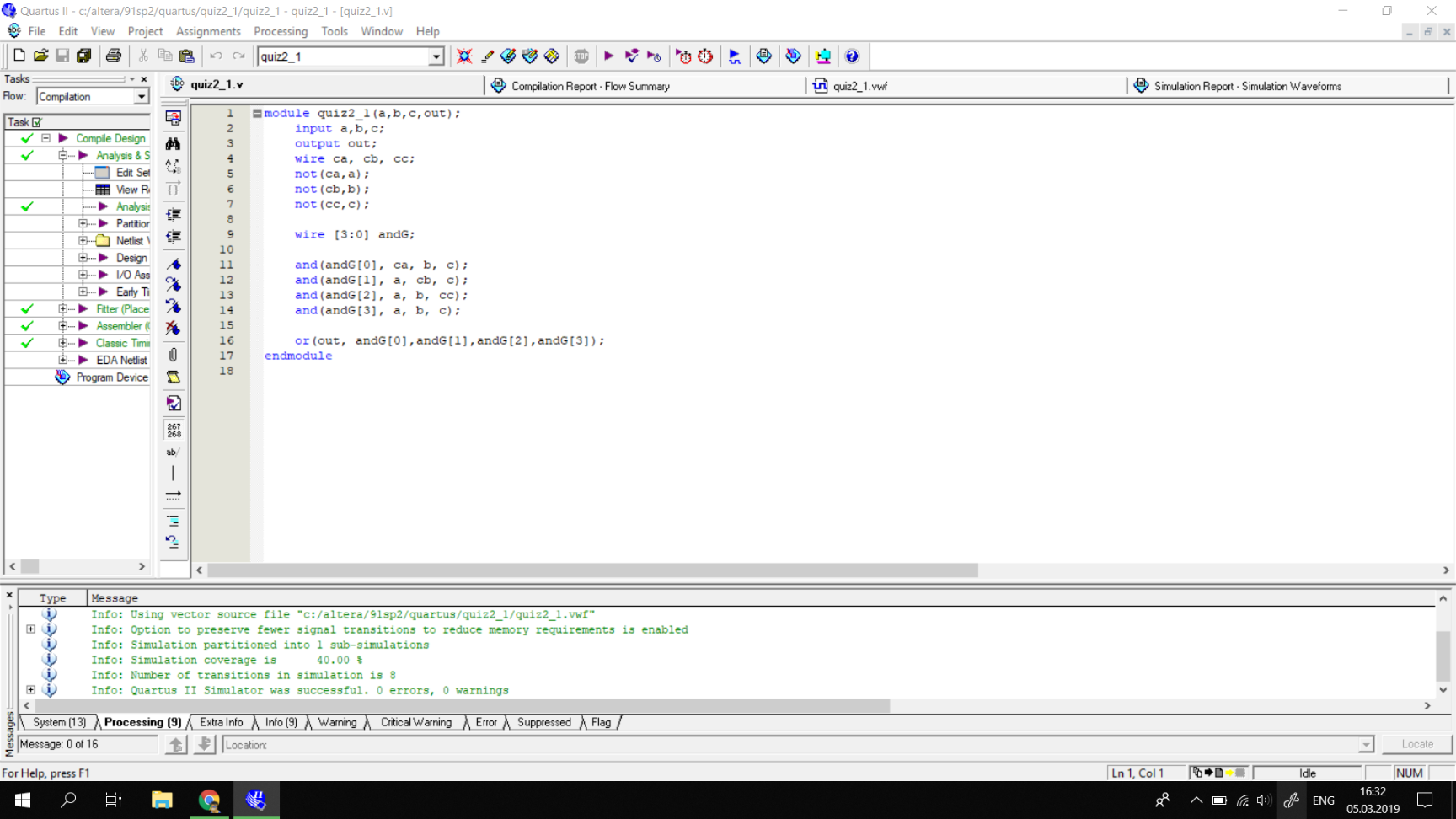
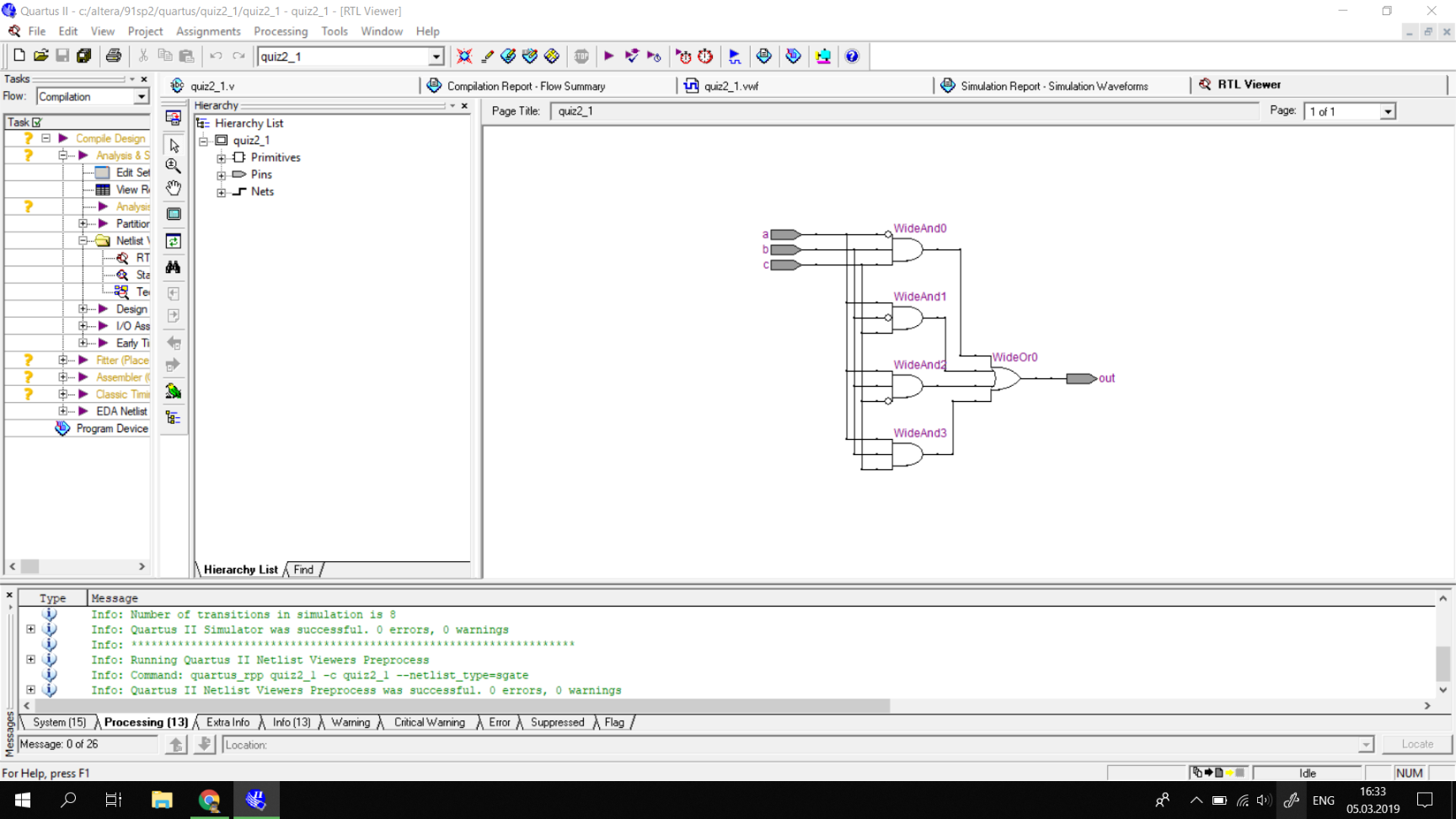
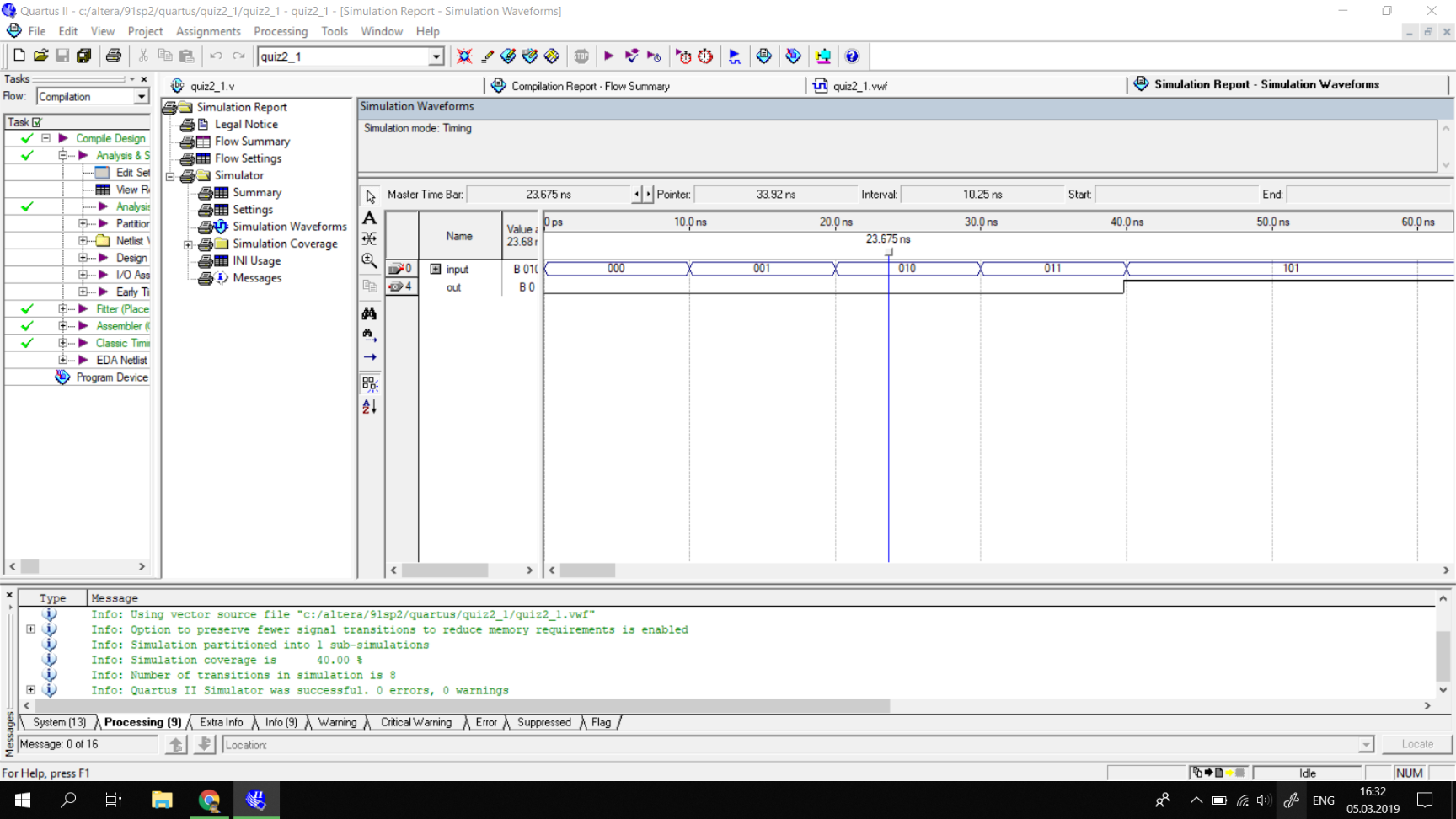
**Task 1**w

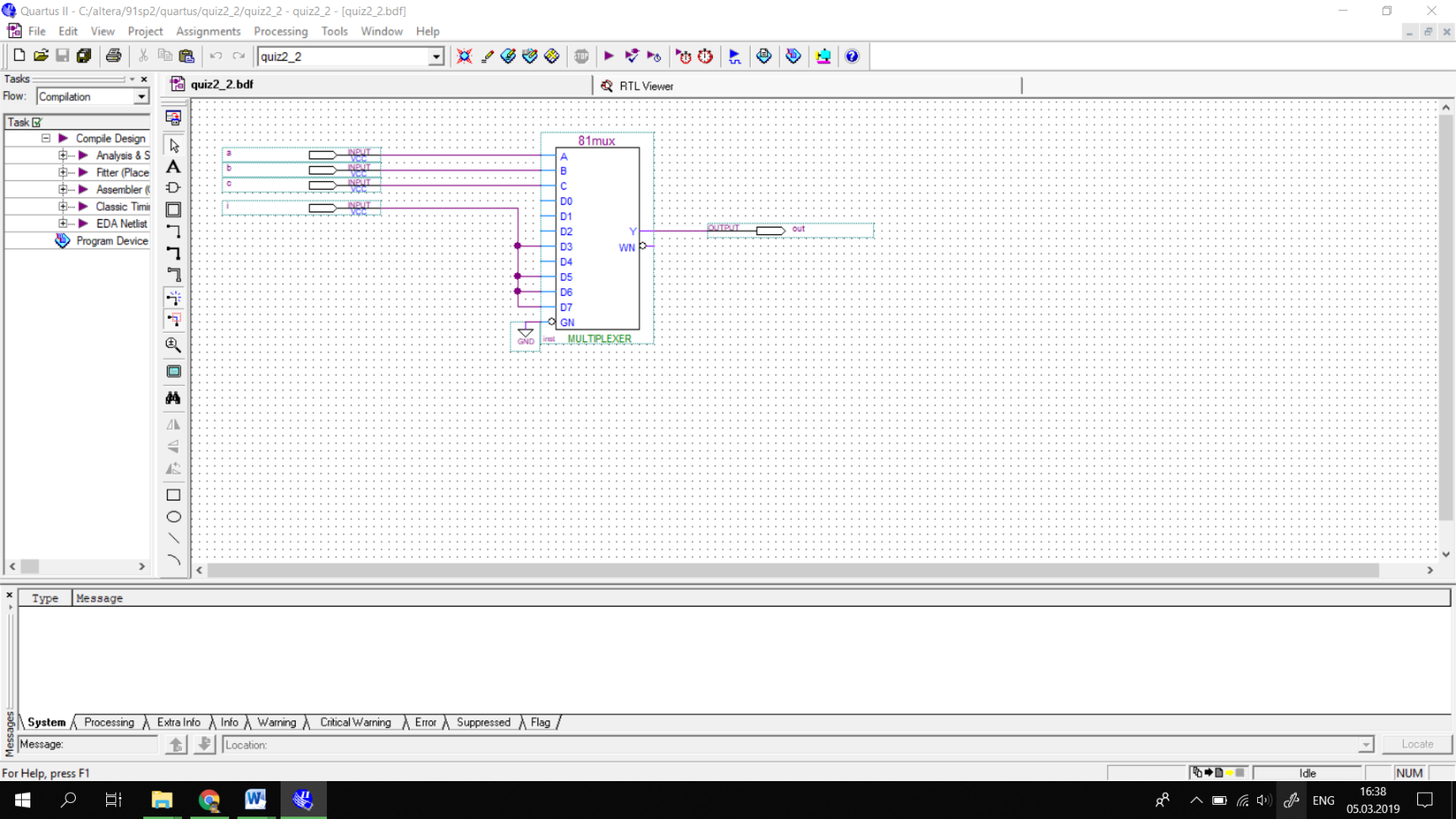
It is part of full adder, which gives the output carry formed by adding the input carry and two bits.

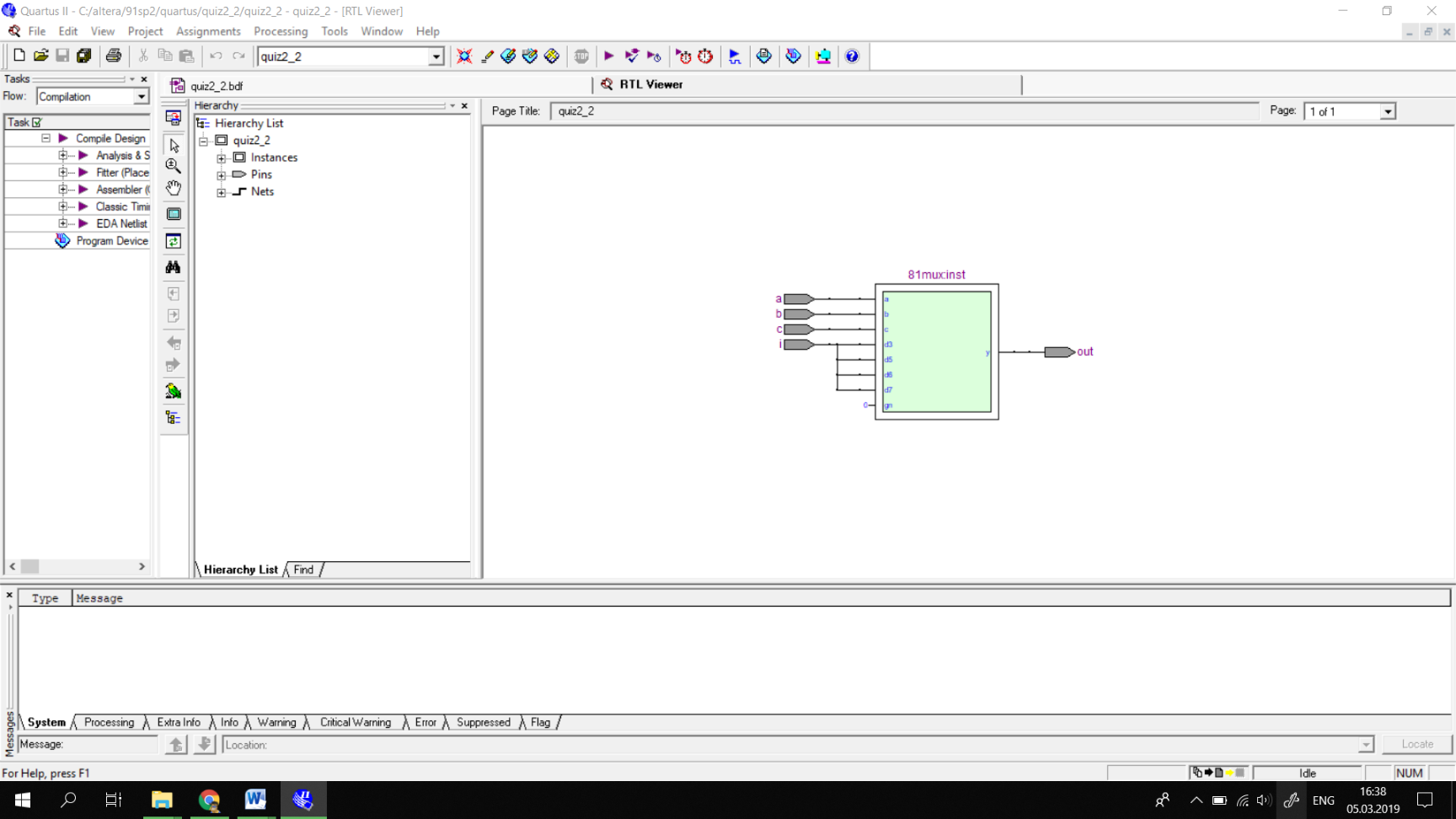
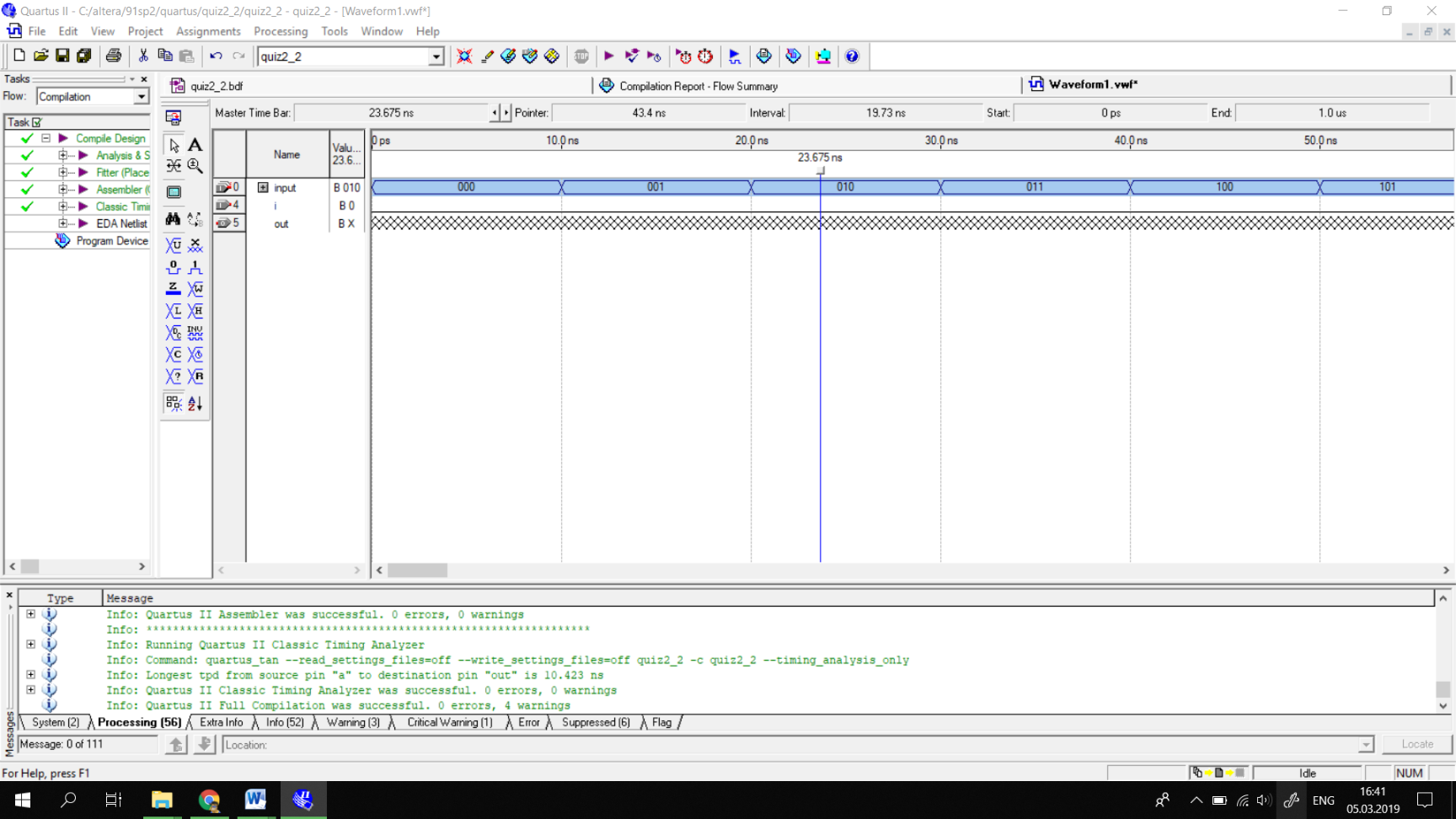
and contains 3 transistors 4 \* 3 = 12

Not contains 1 transistor 3 \* 1 = 3

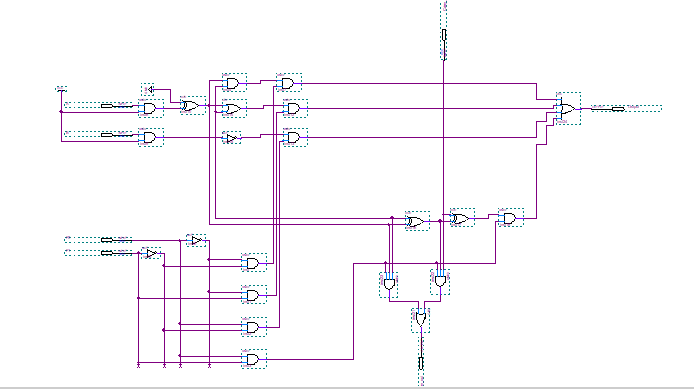
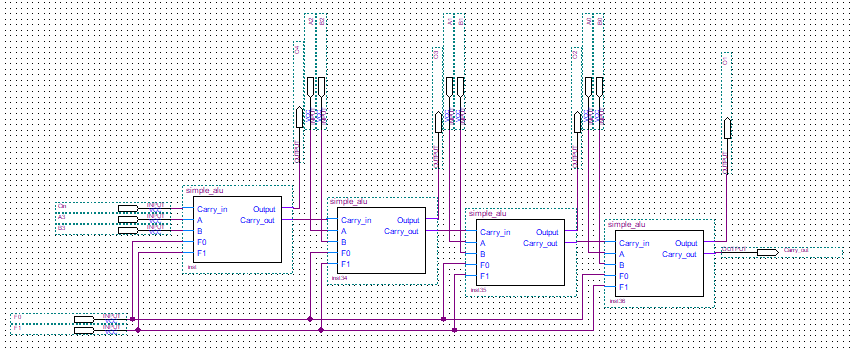
Or contains 4 transistors 1 \* 4 = 4 TOTAL: 12 + 3 + 4 = 19

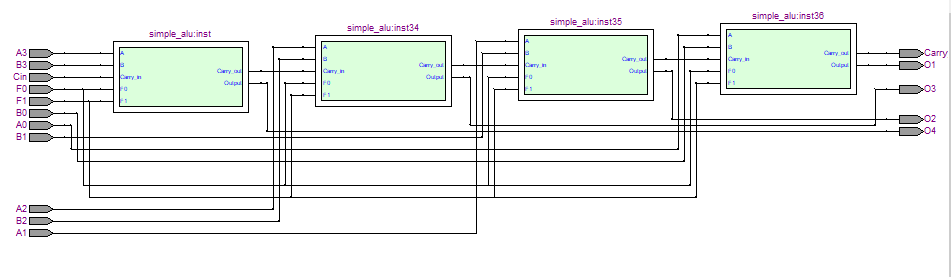
**Task2**

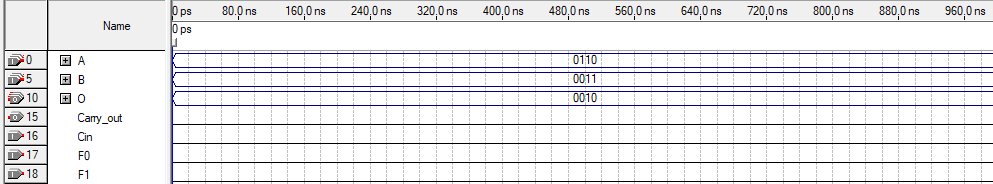
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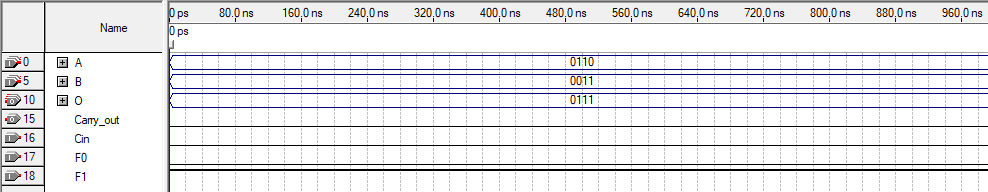
**Task3**



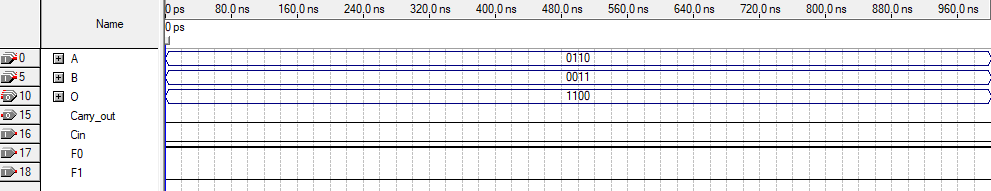




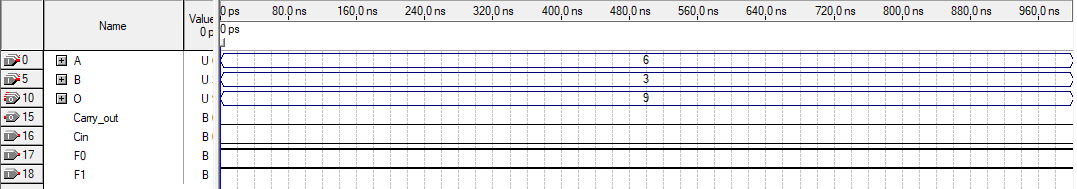
When F0 and F1 are low logical operation AND is performed bit by bit



When F0 is low and F1 is high logical operation OR is performed bit by bit

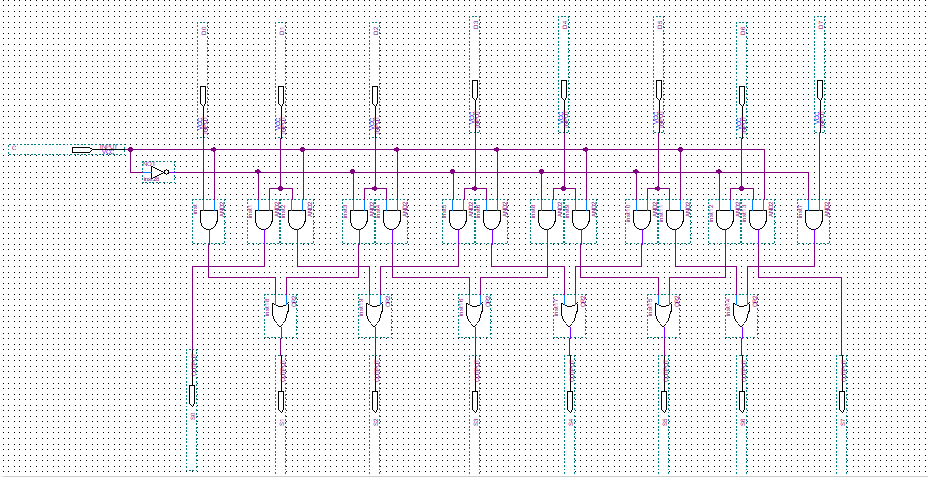


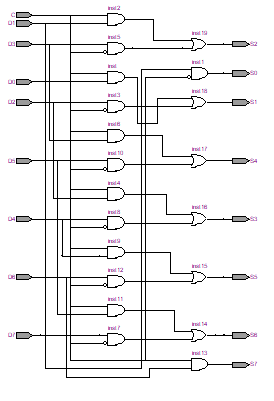
When F0 is high and F1 is low logical operation NOT is performed on B inputs

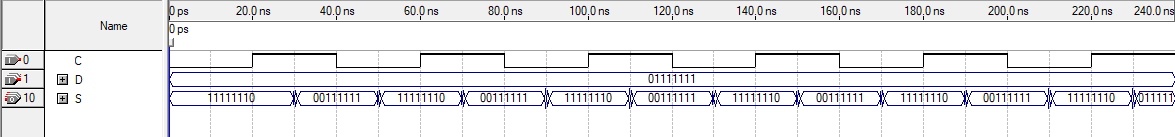


When F0 is high and F1 is high 4 bit Addition is performed

**TASK4**







This combinational circuit shifts the input bits left or right, depending on which control line(C) is high.

**TASK5**

